Biomedical

Low Noise Amplifier

A Project

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by

Anthony Shanks

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Low Noise Amplifier

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Using electrodes to read electrical signals from the human body and display them on an oscilloscope requires an analog front end to properly capture, amplify, and digitize the voltage levels from the electrodes. The first stage of the analog front end is the low noise amplifier (LNA), which is designed to amplify the signal by 40db or more, without adding significant noise. This application also requires the LNA to reject any common-mode noise that may be present on the signal by at least 100db.
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Chapter 1

INTRODUCTION

1.1 Background

One of the most widely used and well-known electronic medical devices is the electrocardiogram (ECG). This device is used to read and graph the tiny electrical signals from the human body which are generated by the heart muscle contractions during each heartbeat. These electrical signals are acquired using electrodes connected between the human body and a device that is designed to provide gain and digitize the signal for processing and display. Due to these signals only being on the order of 1-10mV and the noisy environment these signals must be acquired in, the first stage of this device that provides the gain must be well designed to provide high gain, low noise, and high common-mode rejection. This report presents a low noise amplifier (LNA) that meets these requirements.

1.2 System Level Design

The entire system to acquire, sample, and display electrical signals from the human body comprises many different circuit blocks, with the LNA being the first one on the input of the analog front end (AFE). The rest of the system includes a bandpass filter following the LNA to pass only the frequencies of interest, a variable gain amplifier (VGA) to control how much voltage is needed to supply a suitable amplitude to the analog-to-digital converter (ADC), and finally a successive approximation ADC to digitize our electrical signal for storage and further processing in the digital domain. A block diagram of our overall system design is shown in the following figure.
1.3 Low Noise Amplifier Architecture Choice

The specifications for the design ultimately decide the best architecture to use for the design, so it is necessary to understand the overall process of reading electrical signals from the body. The method of obtaining the electrical signals from the body will be to use standard electrodes as contact points which will directly connect to our biomedical AFE. These signals can have a significant DC offset, and the differential amplitude can be very small; typically on the order of 1mV, with 10mV being at the high end of the range for the signal amplitude. The typical frequencies of interest are in the 10-1000Hz range, as the human body’s waveforms are slow. Due to this low frequency range and the very small signal amplitude, the amplifier bandwidth needs to be kept low in order to keep the input referred noise small in comparison to the input signal amplitude. Another design consideration for this amplifier is the environment in which this biomedical system will be used. Since a hospital is the primary location where this device will be used, the environment will have a tremendous amount of common-mode noise present from other
devices, as well as 60Hz noise from the lighting. This leads to a high common-mode rejection requirement for the LNA, on the order of 100-120dB. With a now complete understanding of the device requirements, we can derive a set of minimum specifications that need to be met by the LNA. The table below outlines these design specifications.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Supply</td>
<td>5V</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>≥40dB</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>70°</td>
</tr>
<tr>
<td>CMRR</td>
<td>≥100dB</td>
</tr>
<tr>
<td>Bandwidth (-3db)</td>
<td>1kHz</td>
</tr>
<tr>
<td>Input Referred Noise (RMS)</td>
<td>≤10µV</td>
</tr>
</tbody>
</table>

Table 1.1 LNA Target Design Specifications

With these design specifications now determined, an exploration of amplifier architectures can be evaluated.

An additional design consideration is the fact that electrodes connect to the human body in different places, so the signal to the biomedical AFE can carry a significant DC offset. Therefore although it is not listed as a specification in Table 1.1, when choosing an amplifier architecture the need to remove a DC offset must be considered. To meet this requirement, a differential difference amplifier (DDA) with AC coupled feedback was considered, as shown in Figures 1.2(a) and 1.2(b). This amplifier architecture sums the output currents from two transconductance amplifiers, and then converts this summed current into an output voltage. Feedback is then applied around the amplifier, but using a coupling capacitor so that the DC gain is unity. This reduces the impact of the dc offset since it is not gained up, so the amplifier output does not saturate. However this does not completely solve the problem since the DC offset voltage present at the input is still present at the output. Since off-chip components are allowed for this LNA design, it was decided that a different amplifier architecture would be used which
includes external input coupling capacitors and bias resistors preceding the LNA, as shown in Figure 1.3.

Figure 1.2(a) Block Diagram for the Differential Difference Amplifier (DDA) [2]

Figure 1.2(b) The AC Coupled Feedback Circuit used with the DDA [2]

Figure 1.3 Amplifier architecture using off-chip AC coupling capacitors
After deciding that there was no inherent requirement for DC offset cancellation in the LNA itself, a standard triple opamp instrumentation amplifier [3] was considered as shown in Figure 1.4. This design has the advantage of being straightforward to implement since only one opamp would need to be designed and instantiated three times in the design, however when doing more research in the literature this was not a very popular design choice. This is due to the fact that many resistors would need to be well matched in the design, along with large amount of silicon area required for the many resistors along with the three separate opamps.

![Figure 1.4 Triple Opamp Instrumentation Amplifier](image)

Although this solution would likely work well in a different application where discrete components and “off the shelf” opamps could be used, it was decided not to pursue this architecture for an integrated amplifier intended to be used on chip for our biomedical AFE. An alternative architecture was instead pursued that is commonly implemented on chip in many IEEE publications [4,5,6]. This led to the choice of the Current Balancing Instrumentation Amplifier (CBIA) [1]. This architecture is commonly used in integrated designs, with good results. In particular the CBIA architecture is well suited for use as a biomedical front end
amplifier with similar requirements to what are needed for this design. A simplified conceptual diagram of a CBIA amplifier is shown in Figure 1.5.

![Current Balancing Instrumentation Amplifier Block Diagram](image)

**Figure 1.5 Current Balancing Instrumentation Amplifier Block Diagram**

In this type of instrumentation amplifier, the differential input drives a transcondutance stage, whose output current is proportional to the input voltage divided by the resistor value, $R_g$. The output current of this transconductance stage feeds into a current mirror stage that mirrors the current $I_g$ to the output stage. The output stage is comprised of a transresistance stage, which generates the output voltage of the amplifier by driving the amplifier output to match the input current $I_s$, but through a much larger resistance noted in the figure as $R_s$, which sets the voltage gain as the ratio of $\frac{R_s}{R_g}$. The CBIA architecture achieves this gain using only the two resistors shown in the figure, greatly reducing the matching requirements of the design. The only requirement is that the ratio of these two resistors only varies slightly, as the ratio of $R_s$ and $R_g$ determines the closed loop gain.
Chapter 2

Design of the Low Noise Amplifier

2.1 Design Overview

The overall philosophy for this amplifier design was to achieve high gain while adding very little self-generated noise, and the large transistors sizes used heavily reflect this requirement. All of the transistors in the entire signal path use long channel lengths and large gate widths, to achieve the large gate areas required to keep the $\frac{1}{f}$ noise they contribute to a minimum.

As mentioned in the specifications shown in Table 1.1, amplifier bandwidth was limited to keep the total integrated noise low. This is acceptable since the biomedical signals used in this application only have a bandwidth of about 10-1000 Hz. The following sections will describe in detail the different parts of this amplifier, as there are several different stages in this circuit employing multiple feedback paths.

The top level design of this circuit includes three main parts which are called the input stage, the current mirror stage, and the output stage. An overview showing all of these stages is shown in Figure 2.1. The input stage is comprised of a PMOS differential pair with an NMOS load, biased using two PMOS cascode tail current sources whose inputs come from the current mirror stage. In the input stage, the resistor $R_g$ is connected between the sources of the input transistors to convert the differential input voltage to a differential current. The output of the first stage is input to the second stage, which is a feedback amplifier with a cascode current source output. This second stage is called the “Current Mirror stage” here, because it’s output is both fed back to the tail current sources in the first stage and mirrored to the 3rd stage. The input nodes of this second stage feedback amplifier will be driven to have a differential input signal nearly equal to zero when a current equal to the signal current $I_g$ generated from resistor $R_g$ is fed back from the second stage into the input stage, thus restoring current balance. That is, the two tail current
sources in the first stage are intentionally imbalanced by the feedback from the second stage, so as to cancel out the signal current $I_g$ and cause the input transistor bias currents to once again be equal. This “Input Stage”-“Current Mirror” feedback path is the first key part of how the overall amplifier works.

The second part of the operation of this amplifier is what happens after this same current $I_g$ is also mirrored to the output stage as $I_s$. The output stage that the current is being driven into is exactly the same as the input stage, except the resistor connected between the sources of the differential pair is much larger, and is what sets the voltage gain. The outputs of the output stage are at the gates of this stage’s input differential pair. In this stage, since the resistance is much larger, in order to balance the tail currents the signal voltage input to the differential pair needs to be much larger. In fact, the differential input signal to this stage is directly proportional to the
output stage resistor $R_s$ divided by the input stage resistor $R_g$. Therefore the voltage gain of the overall amplifier is given by the following equation:

$$\frac{V_{out}}{V_{in}} = \frac{R_s}{R_g}$$

Equation 2.1

In the output stage, the signal voltage input to the differential pair transistors is used to restore current balance. However unlike the input stage, the mechanism which forces this balance is an auxiliary amplifier that directly drives the gates of the output stage differential pair, with the inputs to the auxiliary amplifier being the outputs of this amplifier, similar to the input stage. Feedback forces the differential input signal to the auxiliary amplifier to be nearly zero, which in turn forces the tail current sources in the output stage to be unbalanced and cancel out the signal current flowing in the resistor $R_s$.

Now that the overall amplifier operation has been discussed, a full schematic of the design is shown in Figure 2.2 and the individual components will be discussed.
One of the requirements of the low noise amplifier is that from input to output the signal path is fully differential. Therefore, common-mode feedback circuits drive the common-mode output voltages of the input stage and the output stage to be equal to a common-mode reference voltage. This is accomplished by adjusting the bias currents flowing in the NMOS load transistors in each stage. The same common-mode feedback circuit is used for both the input stage and the output stage, and is shown Figure 2.3.

This common-mode feedback circuit utilizes a dual differential pair design that compares each of the single-ended output voltages of the amplifier to a common-mode reference voltage, and then sums the currents from these two differential pairs into the input of an NMOS current mirror. This current mirror provides the bias to the NMOS load transistors in the amplifier. For this feedback circuit to operate properly, the input transistors in both differential pairs must
remain turned on and in saturation across the entire output voltage swing of the main amplifier. To ensure this is true, the differential pair transistors M5, M6, M12, and M13 must have a sufficiently large $V_{on} = V_{gs} - V_t$, which requires a small $\frac{W}{L}$. This is why relatively large channel lengths and small gate widths were used for these input pairs, which departs from what was done for the rest of the design. However, after the design cycle was complete and while looking for potential improvements, it was noted that the large $V_{on}$ requirements used here could be lowered quite a bit due to the needs of this specific application. Since the output nodes of the input stage and output stage amplifiers (where these common-mode feedback circuits are used) are designed to be driven to zero volts differential, there is no real need for a large voltage swing on these nodes. Only that they can support a specified common-mode voltage and then swing a few tens of mV up or down from that particular bias point.

The auxiliary amplifier that drives the inputs of the differential pair in the output stage is a simple single stage fully differential amplifier. The full schematic of this amplifier including it’s common mode feedback circuit is shown in Figure 2.4.
Since this auxiliary amplifier is designed to drive the inputs of the output stage differential pair, it is required to also be fully differential from input to output, and so needs its own common-mode feedback. The common-mode feedback circuit used for this auxiliary amplifier is the same type of common-mode feedback used for the input and output stages, however the device sizes and the overall design considerations are different. The $V_{on}$ required for the common-mode feedback differential pair transistors is much larger than it is for the input and output stages since the transistors in this common-mode feedback circuit need to remain on and in saturation over the entire output voltage swing of the output stage. Therefore, the transistor $\frac{W}{L}$ were designed as small as possible to maximize the available output voltage swing. This is important due to the fact that the closed loop gain is on the order of 40db, so the output voltage swing can be as high as several volts. The transistor $\frac{W}{L}$ ratios were made small by using long channel lengths of the devices. However there is a limitation on how long the channel lengths can be made due to stability concerns raised when too much capacitance is added to the amplifier output, as these nodes already have to drive a lot of capacitance in this design.

The entirety of this circuit includes multiple feedback paths; therefore the circuit can potentially startup with invalid bias conditions that can force the circuit out of its allowed operating conditions. Spice simulations have confirmed that this problem can occur for this circuit. To ensure that the amplifier starts up in an allowed operating region, a startup circuit is included which shorts the outputs of the amplifier and then releases them after a certain amount of time to allow for the circuit to bias up correctly before applying feedback to the output stage. The startup circuit used by this LNA is shown in Figure 2.5.
Figure 2.5 Startup Circuit Schematic
This startup circuit is designed to mirror a bias current and use it to charge a MOS capacitor to provide the needed time delay. When the voltage on the MOS capacitor gets high enough, that will disable the pull down MOSFET switches connected to the output nodes of the amplifier. The time required to charge the MOS capacitor provides the needed delay between the time when power is first turned on and when the final feedback loop is closed. The startup circuit includes some programmability of the delay time, along with a multiplexer with override capability to be able to manually toggle the shorting switches on and off. This was included as a backup option in case the startup circuit fails or the included programmability in the startup time is insufficient in some cases.

2.2 Electrode DC Offset Removal

As mentioned previously, due to the nature of the electrode connections to the biomedical AFE, there is often a large DC offset present at the input of the LNA. Without any kind of DC offset removal circuit, this would completely saturate the amplifier output due to the high gain. Instead of handling this DC offset removal on chip, an external single pole high pass filter will be added outside of the chip before the input pads. It is important for this circuit to have a high input impedance and a low enough cut off frequency to not significantly attenuate the low frequency signals that can be produced by the human body. A schematic of the final high pass filter is shown in Figure 2.6 using commonly found off the shelf capacitor and resistance values. The component values chosen will result in a cutoff frequency of about 3Hz, which is well below the required frequency range for this application.
This completes a comprehensive review of the entire design including details of all of the circuit blocks that comprise the LNA. In the next section, all of the performance metrics for this circuit will be shown in detail along with a review of the simulation results.
Chapter 3

Simulation Results

3.1 Final Pre-layout Simulated Design Specifications

Prior to evaluating the simulated performance and waveforms, the simulation testbench needs to be understood. Figure 3.1 shows the simulation testbench schematic.

![Figure 3.1 Top Level Testbench Schematic](image)

The ideal input sources in the testbench are the input voltages connected to the LNA and the 25µA bias bias current that will be delivered to the LNA using an on-chip reference circuit included as part of the overall AFE. To model the loading of the next stage in the AFE on the LNA, ideal load capacitors are used. The additional capacitors shown in Figure 3.1 are to provide frequency compensation for the LNA. Due to their large values, these capacitors will be included off-chip. These component values are summarized in Table 3.1. In addition, the values for the resistors included inside the LNA which set the value of the voltage gain, $R_g$ and $R_s$, are also given in Table 3.1. After the final LNA circuit was simulated, the results shown in Table 3.2 were obtained.
<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rg</td>
<td>2500Ω</td>
</tr>
<tr>
<td>Rs</td>
<td>350kΩ</td>
</tr>
<tr>
<td>cload</td>
<td>1pF</td>
</tr>
<tr>
<td>cc1</td>
<td>500pF</td>
</tr>
<tr>
<td>cc2</td>
<td>10nF</td>
</tr>
</tbody>
</table>

Table 3.1 Component Values Used in the Testbench

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain</td>
<td>39.84dB</td>
</tr>
<tr>
<td>Maximum Voltage Swing</td>
<td>2Vpp</td>
</tr>
<tr>
<td>Bandwidth (-3dB)</td>
<td>1.4kHz</td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td>6.19µV</td>
</tr>
</tbody>
</table>

Table 3.2 Results Obtained By Simulation

3.2 Transient Response

Figure 3.1 shows the startup characteristics of all of the feedback nodes in the circuit as well as the amplifier differential output voltages, named voutp and voutn. The feedback nodes shown (nbias1, nbias2, nbias3, nbias4) are the outputs of the common-mode feedback circuits, and the node named vbias is the internal common-mode feedback node of the auxiliary amplifier. The default startup time was used for this simulation, but the option exists to approximately double the amount of startup time depending on how the configuration bits are set. Figure 3.2 shows the large signal step response of the LNA after the circuit bias has stabilized, with an output step size close to the maximum available output swing. It is seen from this plot that there is no overshoot or ringing at the output or on any of the feedback nodes. This matches well with the simulated AC response for each feedback path, as each phase margin is between 80° to 90°. Figure 3.3 shows the common-mode step response, in which the differential input equals zero, but the common-mode is stepped from one value to another. Figures 3.4 and 3.5 show the amplifier’s response to both sinusoidal and triangle wave inputs.
Figure 3.1 LNA Startup Transient Response
Figure 3.2. LNA Differential Step Response
Figure 3.3. LNA Common-mode Step Response
Figure 3.4. LNA Transient Response with a Sinusoidal Input
Figure 3.5. LNA Transient Response with a Triangle Input
3.3 AC Response

The open loop AC responses for all of the feedback paths of the LNA were simulated to determine the stability of each feedback loop, using AC/DC resistors to break the loop and inject an AC signal voltage. Figure 3.6 shows the open loop AC response of the common-mode feedback circuit in the input stage. The feedback was broken on the node named cmfbout1 and an AC signal was injected into the gates of the NMOS load devices, M22 and M23. Figure 3.7 is the open loop AC response of the similar common-mode feedback circuit in the output stage. The open loop AC response of the feedback path from the current mirror stage to the input stage is shown in Figure 3.8. This feedback path was broken differentially using the same AC/DC resistor method, however the AC signal was injected into the path differentially. Figure 3.9 shows the open loop AC response of the auxiliary amplifier driving the differential inputs of the output stage. This feedback loop was also broken differentially in the same way that the current mirror to input stage feedback loop was analyzed. The closed loop AC frequency response of the complete LNA is shown in Figure 3.10. It is interesting to note from this plot that at approximately 1 MHz there is a very quick drop and then rise in gain, indicating that there is a pole and a zero very close together near that frequency. Although this is well outside the bandwidth of the amplifier, it is something worth further investigation to understand where in the circuit this pole and zero occur. Figure 3.11 shows the common-mode rejection ratio of the LNA, which was obtained by placing a common-mode AC voltage source at the input terminals to the LNA. The input and output noise across frequency is shown in Figure 3.12. It is interesting to note that this plot shows a large spike in input referred noise at approximately the same frequency where the pole/zero combination was observed near 1 MHz. This also warrants further investigation.
Figure 3.6 Open Loop AC Response for the CMFB loop used in the Input Stage
Figure 3.7 Open Loop AC Response for the CMFB loop used in the Output Stage
Figure 3.8 Current Mirror to Input Stage Open Loop AC Response
Figure 3.9 Auxiliary Amplifier to Output Stage Open Loop AC Response
Figure 3.10 LNA Closed Loop AC Frequency Response
Figure 3.11 LNA Common-mode Rejection Ratio
Figure 3.12 LNA Input and Output Referred Noise
Chapter 4

CONCLUSION

After going through the process of designing a low noise amplifier using the current balancing instrumentation architecture, I have learned that although the design requirements are straightforward (high gain with low noise), the implementation details can be complex. The implementation used in this LNA uses many different feedback paths, and that combined with the large devices that are required to meet the low noise requirement can make it difficult to achieve good phase margins. The many feedback paths can also cause potential issues with circuit startup, which is why a separate startup circuit was included in this design. Even with those complications, this architecture does provide a high amount of gain, low noise, and high CMRR, so it is suitable for use as a high performance amplifier for an ECG analog front end. There are, however, a few design changes that can be explored to improve this circuit. Since this is a low noise, low bandwidth design it is expected to be large in area. However it should be possible to reduce the amount of area used for both the startup circuit and common-mode feedback circuits. The startup circuit could be completely replaced by a counter assuming that a low frequency clock is available. This would eliminate the need for the large MOS capacitor and the current mirrors in the startup circuit. In the common-mode feedback circuits, the differential pair device sizes could be reduced since the inputs to these feedback circuits are expected to only have a small signal swing. Another needed improvement for this design is to understand where in the circuit the pole/zero pair seen in the closed loop AC response is coming from, and reduce or eliminate it.
REFERENCES


