A CURRENT-MODE LOGIC FREQUENCY DIVIDER FOR
AN ALL DIGITAL PHASE-LOCKED LOOP IN 0.18UM CMOS

A Project

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Abstract

of

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Sruthi Penmetsa

A phase-locked loop (PLL) is an important mixed-signal circuit that is used on almost every integrated circuit. A frequency divider is needed in the PLL loop to allow the use of a low frequency reference clock that is typically provided by a highly accurate off-chip crystal oscillator. This project is focused on the design of a current-mode logic (CML) frequency divider in 0.18um CMOS for an all digital phase-locked loop. Current-mode logic is used for the first few stages of the overall frequency divider, where the frequency of operation is too high for standard CMOS logic to operate properly.

For this project, a CML frequency divider was designed in 0.18um CMOS and simulations were performed to verify performance for typical as well as worst case conditions.

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Date

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Chapter 1

INTRODUCTION

1.1 Background

A phase-locked loop (PLL) is a negative feedback system that generates an output clock whose phase and frequency are synchronized with a reference clock. Phase-locked loops are key mixed-signal circuits that are used in many different integrated circuits for clock and data recovery, modulation and demodulation of communication signals and frequency synthesis to create clocks with different frequencies. As shown in Figure 1, a typical PLL consists of a phase frequency detector (PFD), a low pass filter (LPF), a voltage controlled oscillator (VCO) and a frequency divider. [2]

![Figure 1. Block diagram of a typical PLL](image-url)
In a typical phase-locked loop the phase frequency detector has two inputs, one for the input reference clock and the other for the VCO clock after it has been reduced to the frequency of the reference clock by the frequency divider. The PFD compares the phase and frequency of these two input signals and outputs a signal whose average value is proportional to the phase difference between the two input signals. The low pass filter removes any high frequency components from the signal and feeds the result into the control input of the voltage controlled oscillator to control the frequency of oscillation. The output from the VCO is input into the frequency divider, which is used to reduce the frequency of the VCO clock to match the frequency of the reference clock. This is necessary since the frequency of the on-chip clock created by the VCO is typically much higher than the frequency of the reference clock, which is usually provided from off-chip using a highly precise crystal oscillator. The frequency divider circuit is usually made up of a Current-Mode Logic (CML) divider followed by a CMOS divider. The CML divider is used at the output of the VCO where the frequency of the clock is typically too high for flip-flops built using standard CMOS logic to operate. After the CML divider has reduced the clock frequency low enough for standard CMOS logic to function properly, then the clock frequency is further reduced to the reference frequency by using a second frequency divider employing standard CMOS logic flip-flops.
1.2 All Digital Phase-Locked Loop

A digital phase-locked loop is used for the same applications as a traditional analog phase-locked loop, but with as many analog circuits in the PLL as possible replaced by digital circuits. Due to a majority of the circuits being digital, an all-digital phase-locked loop (ADPLL) is smaller, has lower power consumption, and is more robust as compared to a traditional analog PLL [3]. The block diagram of an ADPLL is as shown in Figure 2.

![Figure 2. Block diagram of an all-digital PLL [5]](image)

In an ADPLL, the PFD performs the same function as it does in a traditional PLL, which is to compare the phase and frequency of the frequency divided DCO clock to the reference clock. The time-to-digital converter then converts this phase difference into a digital code, which is averaged using a digital low pass filter. The DCO is an oscillator whose frequency is controlled using the digital control bits from the digital low pass filter.
The frequency of the DCO output clock is reduced to the reference clock frequency using the CML and CMOS frequency dividers.

1.3 Current-Mode Logic Frequency Divider

The CML frequency divider is one of the most challenging designs in the phase-locked loop due to the high frequencies at which it must operate. The focus of this project is to design a CML frequency divider for an all-digital PLL in 0.18um CMOS, whose DCO operates at a nominal frequency of 1.8 GHz.
Chapter 2

DESIGN OF THE CML FREQUENCY DIVIDER

2.1 Circuit Description

A current-mode logic (CML) frequency divider is needed at the output of the DCO where the clock frequency is too high for standard CMOS logic flip-flops to operate. Since CML circuits consist of only NMOS transistors and resistors, and use limited voltage swings for their input and output signals, these circuits are much faster than standard CMOS logic circuits which use slower PMOS transistors. In this project fully-differential CML logic is used to build toggle flip-flops to divide the DCO clock frequency by a factor of 4. The DCO frequency range is 1.5 GHz – 2.0 GHz [6], so after the CML divider reduces the clock frequency by a factor of 4 the highest frequency that the CMOS divider needs to operate at is 500 MHz. The output of the CML frequency divider is then fed into the CMOS divider for further frequency division, to reduce the output clock frequency from the CML and CMOS frequency dividers to match the reference clock frequency.

Each CML toggle flip-flop divides the input clock frequency into half its value. The CML toggle flip-flop is built by combining a CML D flip-flop with an extra CML buffer with the Q-bar output fed back to the D input. This extra CML buffer is needed to slightly delay the signal in order to avoid errors due to flash through [1]. A schematic of a minimum size CML buffer is shown in Figure 3. This buffer uses a 200uA tail current together with a 3kOhm load resistor to create an output voltage swing of 600mV peak-to-peak on each of the Vop and Von outputs, for a total differential output swing of 1.2Vpp. A schematic
of the CML toggle flip-flop designed based on this buffer which was used for this project is shown in Figure 4.

2.2 CML-to-CMOS Converter

The output of the CML frequency divider is a limited swing differential voltage, not rail-to-rail CMOS digital logic levels. In order to output a full CMOS logic swing from 0V to 1.8V, a CML-to-CMOS converter was added to the output of the CML frequency divider. The output of this converter can be then input to a standard CMOS digital logic frequency divider to complete the needed frequency division. The CML-to-CMOS converter is shown in Figure 5, and a top-level schematic of the entire CML frequency divider including this converter is shown in Figure 6. Figure 7 shows the simulation test bench used for the complete CML frequency divider.
Figure 4. CML toggle flip-flop schematic
Figure 5. CML-to-CMOS converter schematic
Figure 6. CML frequency divider schematic
Figure 7. CML frequency divider test bench
Chapter 3

SIMULATION RESULTS

Figure 8 shows the differential input and output waveforms for the CML frequency divider. Since the maximum output frequency from the DCO is 2 GHz, that frequency was used for the input to the CML frequency divider. The CML frequency divider consists of two CML toggle flip-flops in series, each of which divides the frequency in half. So the frequency of the output is the input frequency divided by four. The output frequency is 500 MHz, making the period of output clock equal to 2.0 ns. This output frequency is low enough to be further reduced using a second frequency divider which is made up of standard CMOS logic flip-flops.

In Figure 8, the signal “Vdm_1” is the differential output of the first CML toggle flip-flop and the signal “Vdm_2” is the differential output of the second CML toggle flip-flop. The output of the entire CML frequency divider, along with the CML-to-CMOS converter, is shown in Figure 8 as the signal “CLK_cml”. This CLK_cml signal is directly connected to the standard CMOS logic frequency divider which follows. The simulation results shown in Figure 8 are for the typical-typical corner (typical NMOS and PMOS FETs, nominal supply voltage of 1.8 V and nominal temperature of 25°C). The simulation results shown in Figure 9 are for the worst case corner (slow NMOS and PMOS FETs, low supply voltage of 1.6 V and high temperature of 85°C).
Figure 8. Input and output waveforms for the CML frequency divider at the tt corner
Figure 9. Input and output waveforms for the CML frequency divider at the ss corner
Chapter 4

CONCLUSIONS

The design a current-mode logic (CML) frequency divider in 0.18um CMOS for a digital phase-locked loop was successfully completed. As a part of this project, a CML buffer, a CML toggle flip-flop and a CML-to-CMOS converter have been designed and simulated. The maximum input frequency of 2 GHz from the DCO is divided down to 500 MHz using 2 stages of CML of toggle flip-flops. The next step would be to implement this design as part of an overall phase-locked loop on an integrated circuit.
REFERENCES

[1] Dr. Perry L. Heedley, EEE 231 Class Notes, unpublished.


